Remarks

Claims 1-4 are pending in the application without amendment. No new matter has been added.

In the following text, specific references to the present application and the prior art are made using the notation "x:y", where "x" denotes the page or column number, and "y" indicates the line number, within the document being discussed.

Rejections Under 35 U.S.C. § 103(a)

Currently, claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over McTeer (US 5,700,718).

Claim 1 recites:

> A method of constructing a metallization structure on a preexisting dielectric layer of an integrated circuit during fabrication of the integrated circuit, the method comprising the steps of:
> depositing a layer of titanium onto the preexisting dielectric layer of the integrated circuit;
> depositing a layer of aluminum onto the layer of titanium;
> heating the integrated circuit sufficiently to cause the layer of titanium to become at least partially alloyed with the layer of aluminum; and
> further heating the integrated circuit at 400 degrees C for about 45 minutes so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit.

Concerning claim 1, the examiner has indicated that McTeer discloses all of the recited steps of the method except for the step "further heating the integrated circuit at 400 degrees C for about 45 minutes". The examiner indicates, however, that McTeer discloses "further heating the integrated circuit but fails to teach doing the heating at 400 degrees C for about 45 minutes" (Office Action A, 2:25 - 2:26). The examiner states that "since McTeer teaches the further heating for curing the defects, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the heating temperature and the duration through routine experimentation and optimization to obtain optimal curing of defects because the heating temperature and duration are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results...." (Office Action A, 2:27 - 3:5).

McTeer discloses a technique for forming metal interconnections lines with an increased resistance to void formation. (McTeer, 3:22-3:27). McTeer performs an intermediate anneal step of an aluminum layer deposited atop a titanium layer at a temperature greater than 450° C for about 4 to 6 minutes in order to completely react the titanium and aluminum layers to form a single titanium aluminide layer. (McTeer, 4:12-4:17). McTeer then deposits another layer of conducting material atop the newly constructed titanium-aluminide layer such as more aluminum. As a result of the prior formation of the titanium aluminide layer with the intermediate anneal, the overlying conducting material does not substantially react with the titanium aluminide layer. (McTeer, 427-4:30). After depositing a layer of anti-reflective coating on the layer of overlying conducting material, McTeer then performs a final anneal in a furnace at conventional temperatures and for a conventional amount of time. (McTeer, 4:34-4:37).

The Applicant's claimed invention is a method of constructing a metallization structure containing titanium that provides superior contact resistance and electromigration properties while at the same time allowing water, hydrogen, and oxygen trapped in the IC to passivate defects on the surface of a silicon wafer. Titanium is used as a gettering agent. (Specification, 2:1 - 2:2). Gettering reduces the effects of mobile impurities in the silicon and dielectric layers of an IC by restricting the movement of the mobile impurities. As a gettering substance, titanium traps water, hydrogen, and oxygen, thus allowing these substances to be absorbed readily from within the silicon and dielectric layers of an IC. (Specification, 1:18 - 1:27).

Too much gettering is possible. The presence of some particular types of mobile impurities, in moderate quantities, are actually beneficial to the performance of an integrated circuit. For instance, water and its constituent elements are useful under certain conditions for passivating structural defects within silicon by bonding with the defect sites, thus causing the IC to function more efficiently. In that case, substantial gettering of hydrogen and oxygen may actually be a detriment to the performance characteristics of the IC, resulting in increased leakage current and other impediments to optimal device performance. (Specification, 1:28 - 2:19).

The claimed invention takes advantage of the desirable

electromigration and contact resistance properties of titanium, while at the same time limiting its gettering capabilities. Consequently, a sufficient amount of mobile impurities, such as water and its constituent components hydrogen and oxygen are then available to passivate structural defects in the silicon layer of the IC. (Specification, 3:3 - 3:7). The passivating agents bind with the dangling bonds of structural defects 7, thereby inhibiting the ability of the dangling bonds to provide a path for leakage current within silicon layer 10. (Specification, 6:5 - 6:7).

The advantage of alloying the titanium and aluminum is that the gettering capacity of the titanium is restricted, thus allowing mobile impurities such as water, hydrogen, and oxygen to be available to passivate structural defects in the silicon layer of the IC. At the same time, titanium still helps set the structural texture of the aluminum layer, providing low contact resistance and improved electromigration properties. (Specification, 3:8 - 3:17).

Applicant's Claim 1 recites a step for "further heating the integrated circuit at 400 degrees C for about 45 minutes so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit".

McTeer does not teach or suggest the limitation "so that impurities from the dielectric layer have passivated structural defects within a silicon layer of the integrated circuit" as recited in Applicant's Claim 1. McTeer teaches only that voids formed in the metal stack are reduced as a result of the McTeer's technique (McTeer, 3:45 - 3:51). The reduction of voids in the metallization stack as described in McTeer is not the same as passivating structural defects in the silicon layer of the integrated circuit, as recited in Applicant's Claim 1. In the case of reduction of voids, the size of the voids are made smaller, but the existing reduced voids still have dangling bonds that facilitate electron flow and therefore unwanted leakage current. In the case of passivation, Applicant's invention exploits the mobile impurities to bind with the dangling bonds of the structural defects, thereby reducing leakage current. Therefore, although McTeer states that the wafer undergoes an anneal process such as that of the prior art which is conducted in a furnace at conventional temperatures and for a conventional amount of time, there is nothing in McTeer that teaches or suggests that "impurities from the dielectric layer have

passivated structural defects within a silicon layer of the integrated circuit" as a result of the anneal step. Accordingly, McTeer does not meet this limitation.

Further as recited in Claim 1, McTeer also does not teach or suggest that the wafer anneal process is "at 400 degrees C for about 45 minutes". The Examiner states that it would have been obvious to perform routine experimentation because the heating temperature and duration are result-effective variables. However, as known in the integrated circuit fabrication arts, variables such as heating temperature and duration are often critical to desired outcomes of the process, and even small variations can often result in the differences of properties, composition, and formation of integrated circuits. Accordingly, it cannot be assumed that such a discovery would come as the result of routine experimentation, nor that the desired composition and formation of the integrated circuit would result from the Applicant's claimed invention as claimed in Claim 1.

For the above reasons, the Applicants believe that claim 1 is not made unpatentable by McTeer, and is thus allowable. Also, since claims 2, 3, and 4 depend from claim 1, they incorporate the limitations from independent claim 1 that are missing from McTeer and the prior art. Therefore, the Applicants believe that claims 2, 3, and 4 are allowable as well.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-4 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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